An analysis of aLIGO PD circuit

2025-10-20

We perform a numerical analysis of noise in the Advanced Laser Interferometer Gravitational-Wave Observatory (aLIGO) photodetector demodulation circuit. The analysis examines the complete circuit architecture, including the photodiode bias circuit, notch filters for harmonic suppression, and frequency selector circuits. This work provides a comprehensive understanding of noise sources and their contributions to the overall circuit performance.

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This post builds on a couple of earlier posts of mine, LIGO modulation and RLC filters. In this post we will look into the Advanced Laser Interferometer Gravitational-Wave Observatory (aLIGO)'s photodiode circuit and analyze its noise performance. (Also see a follow up post: An SNR analysis of aLIGO circuit)

The actual circuit in use at the moment is shown in Figure 1, and we will refer to it as *v5* in the following pages as it is the version number.

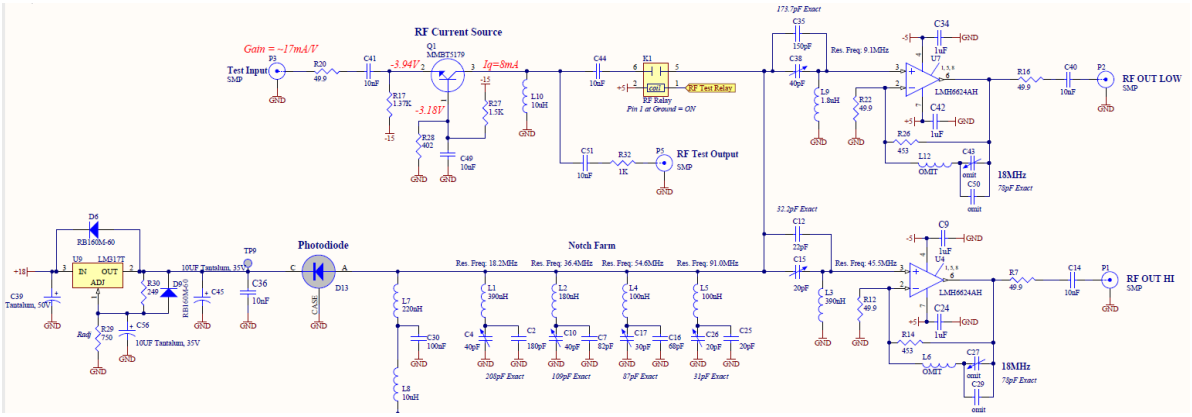

Figure 1: The current circuit used in aLIGO.

Let us take a closer look at the photodiode bias circuit as shown in Figure 2. The diode is under reverse bias, and it will behave as a current source when exposed to light.

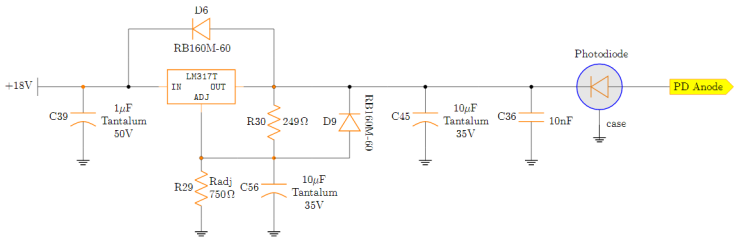

Figure 2: This voltage regulator circuit applies reverse bias to the photo diode.

The output voltage is set to 5V via every electronics hobbyist's favorite LM317T voltage regulator with some reverse bias protection. Note the two parallel capacitors in the output, 10μF and 10nF. The 10nF is a ceramic capacitor which is used to reduce to equivalent serial resistance at higher frequencies to dampen possible oscillations in the output voltage.

The anode of the phododiode is fed into a farm of fine-tuned notches as in Figure 3.

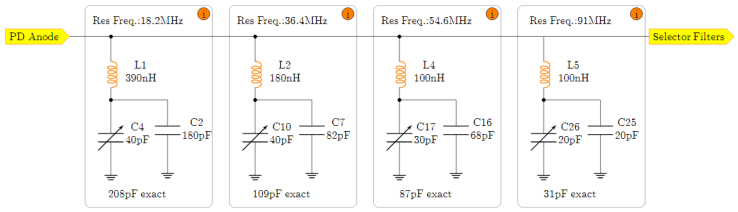

Figure 3: Notch farm to remove various harmonics. Hover over the coils to see their properties. Hover over the info icons to see bode plots … [+] The line continues to frequency selector circuit.

Each block is tuned such that the natural frequency $1/\sqrt{LC}$ is around the target frequency to be carved out. Hover over the info icon, , to see the corresponding Bode plot, and the coils to see their frequency response. In the Bode plot. we just use the series resistance along with the inductance. Skin depth effects and shunt capacitance are not included in the Bode plots. We will certainly include them later.

The selectors are shown in Figure 4.

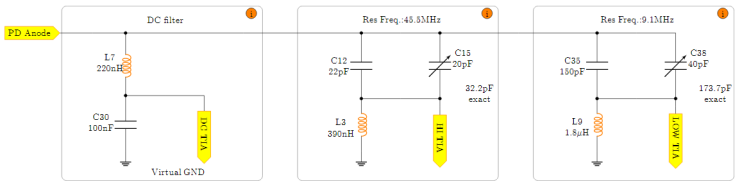

Figure 4: Selector filters. Hover over the coils to see their properties. Hover over the info icons to see bode plots. … [+] The line continues to transimpedance amplifier (TIA).

The Trans-impedance amplifiers (TIA) are shown in Figure 5.

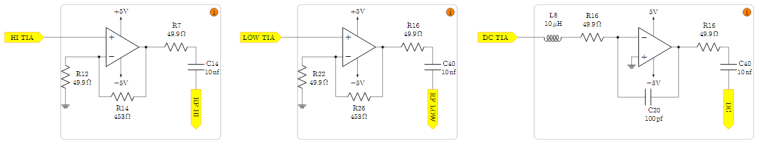

Figure 5: Basic inverting amplifiers with a gain of 10 for the RF outputs.

Table shows the values of the filter elements.

Table 1: The values of the essential circuit elements.

DC readout		9.1MHZ read out		45.5MHz readout		18.2MHz notch		36.4MHz notch		54.6
L7	C30	L9	C35+C38	L3	C12+C15	L1	C2+C4	L2	C7+C10	L4
220nH	100nH	1.8 μF	173.7pF	390nH	32.2pF	390nH	208pF	180nH	109pF	100nH

We build this circuit in LTspice as shown Figure 6 and simulate. The LTspice file can be found here.

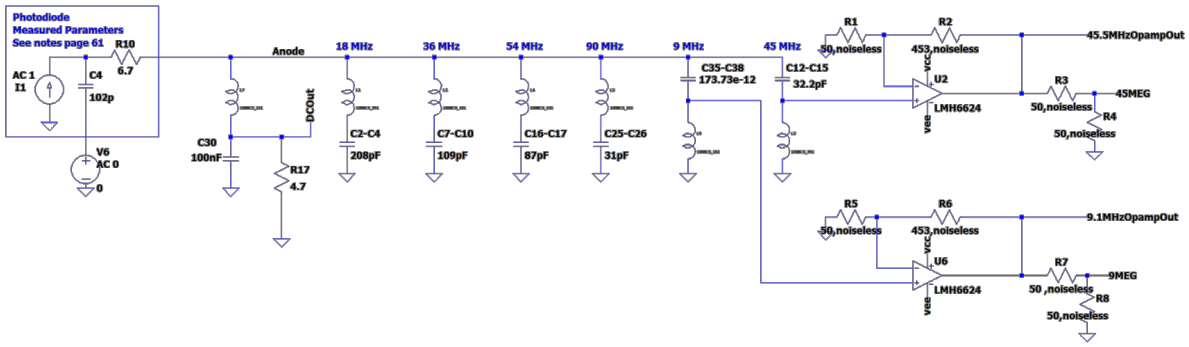

Figure 6: LTSpice circuit for simulation.

We can collect the LTspice simulation data via Python. It is convenient to measure the noise at the OPAMP output in terms its input current equivalent:

$$\text{Equivalent Current Noise} = \frac{(V/\text{gain})^2}{2e}, \tag{1}$$

where the gain is the transimpedance. We plot the noise spectrum in Figure 7.

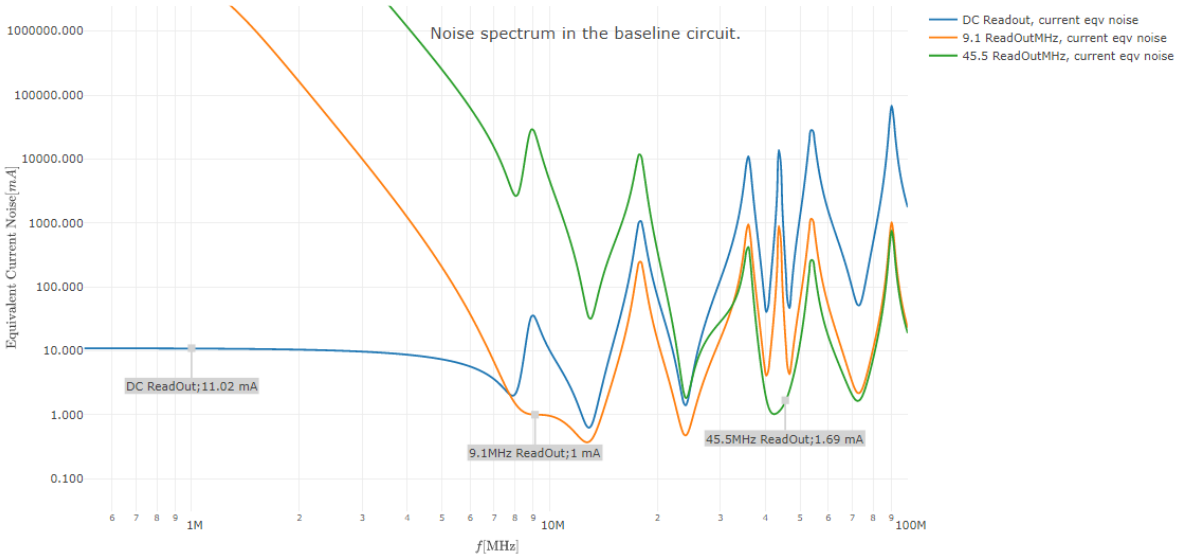

Figure 7: Baseline noise for the readout ports DC, 9.1MHz, and 45.5MHz. The critical values are marked on the plot.

The values annotated in Figure 7 are the values we will want to reduce and they provide us with a benchmark. Can we beat these values and design a circuit with lower noise? That is exactly what we are going to do in following posts. Find a warm up SNR analysis here An SNR analysis of aLIGO circuit